64K X 16 CMOS DYNAMIC RAM WITH FAST PAGE MODE

Document Title

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Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	March 06, 1998	Preliminary
0.1	Modify 40/44L TSOP type II package outline drawing and dimensions notes	June 17, 1998	
0.2	Remove timing waveform of $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle	August 21, 1998	
0.3	Final spec release	September 8, 1998	Final
0.4	Erase t_{CPT} parameter Modify SOJ 40L outline dimensions Modify TSOP 40/44L (type II) outline dimensions	October 23, 1998	

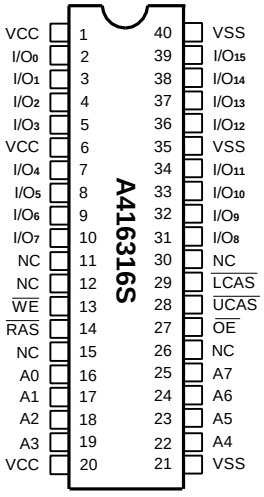
64K X 16 CMOS DYNAMIC RAM WITH FAST PAGE MODE

Features

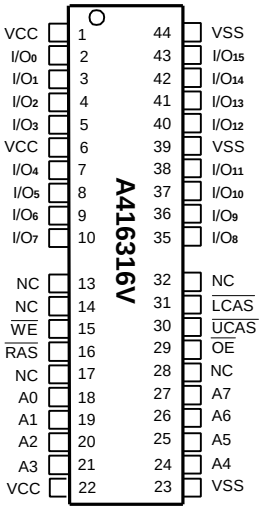
- Organization: 65,536 words X 16 bits
- High speed
  - 40/50/60 ns $\overline{RAS}$ access time
  - 20/25/30 ns column address access time
  - 12/13/15 ns $\overline{CAS}$ access time
- Low power consumption
  - Operating: 160mA (-40 max)
  - Standby: 3 mA (TTL)
- 256 refresh cycles, 4 ms refresh interval
- Read-modify-write, $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, Hidden refresh capability
- TTL-compatible, three-state I/O
- JEDEC standard packages
  - 400mil, 40-pin SOJ
  - 400mil, 40/44 TSOP type II package
- Single 5V power supply/built-in VBB generator

Pin Configuration

■ **SOJ**



■ **TSOP**



Pin Descriptions

Symbol	Description
A0 – A7	Address Inputs
I/O_0 - I/O_{15}	Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe/Upper Byte Control
$\overline{LCAS}$	Column Address Strobe/Lower Byte Control
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VCC	+5V Power Supply
VSS	Ground
NC	No Connection

Selection Guide

Symbol	Description	-40	-50	-60	Unit
t_{RAC}	Maximum $\overline{RAS}$ Access Time	40	50	60	ns
t_{AA}	Maximum Column Address Access Time	20	25	35	ns
t_{CAC}	Maximum $\overline{CAS}$ Access Time	12	13	15	ns
t_{OEA}	Maximum Output Enable ($\overline{OE}$) Access Time	12	13	15	ns
t_{RC}	Minimum Read or Write Cycle Time	75	90	110	ns
t_{PC}	Minimum Fast Page Mode Cycle Time	22	31	40	ns
I_{CC1}	Maximum Operating Current	160	140	120	mA
I_{CC6}	Maximum CMOS Standby Current	2.0	2.0	2.0	mA

Functional Description

The A416316 is a high performance CMOS Dynamic Random Access Memory organized as 65,536 words X 16 bits. The A416316 is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at component and system levels.

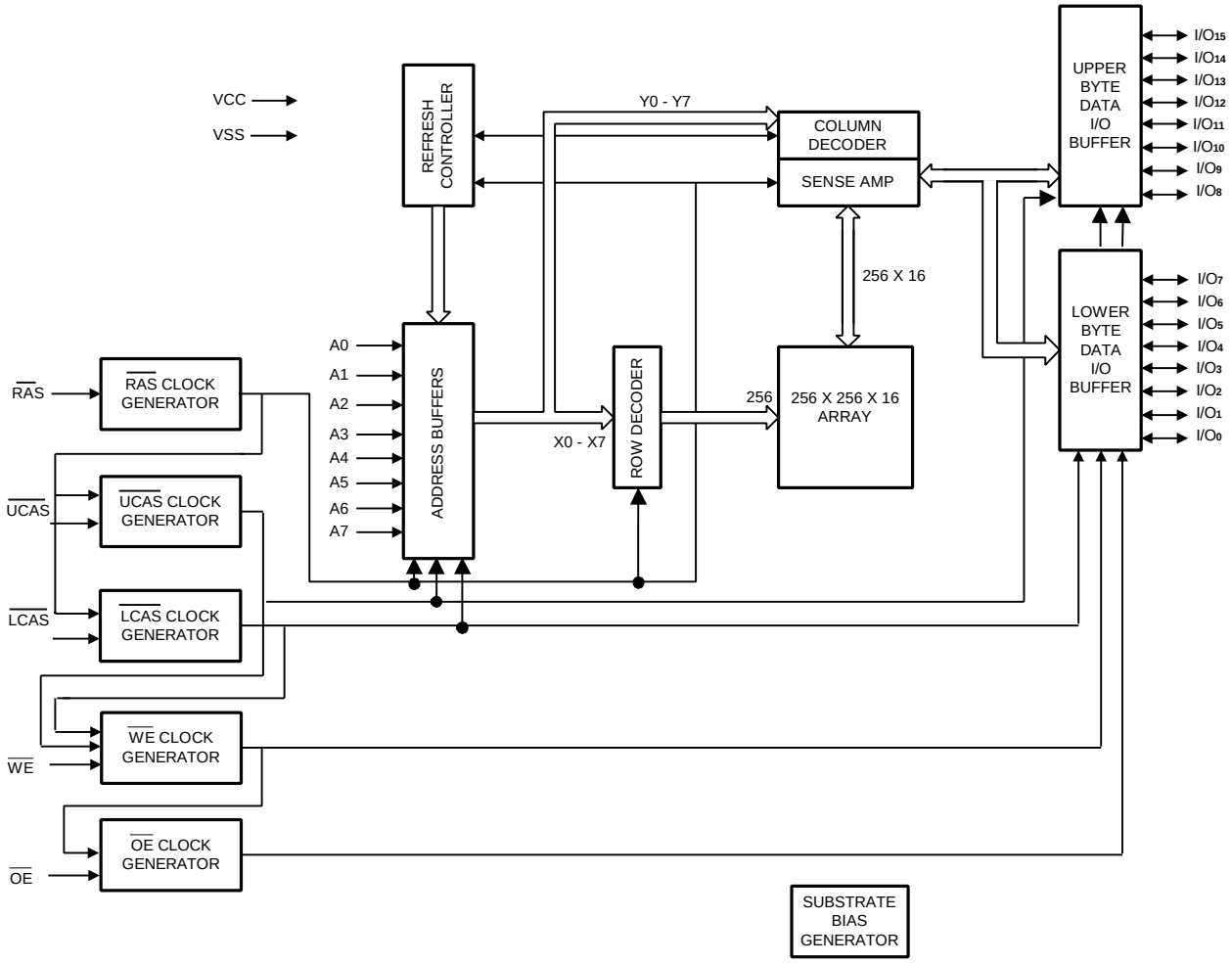
The A416316 features a high speed page mode operation in which high speed read, write and read-write are performed on any of the bits defined by the column address. The asynchronous column address uses an extremely short row address capture time to ease the system level timing constraints associated with multiplexed addressing. Output is tri-stated by a column address strobe ($\overline{UCAS}$ and $\overline{LCAS}$) which acts as an output enable independent of $\overline{RAS}$. Very fast $\overline{UCAS}$ and $\overline{LCAS}$ to output access time eases system design.

All inputs are TTL compatibel. Fast Page Mode operation allows random access up to 256 X 16 bits within a page, with cycle time as short as 22/31/40 ns.

The A416316 is best suited for graphics, digital signal processing and high performance peripherals.

The A416316 is available in JEDEC standard 40-pin plastic SOJ package and 40/44 TSOP type II package.

Block Diagram



Recommended Operating Conditions (Ta = 0°C to +70°C)

Symbol	Description	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
VSS		0.0	0.0	0.0	V
V_{IH}	Input Voltage	2.4	-	VCC + 1	V
V_{IL}		-1.0	-	0.8	V

Absolute Maximum Ratings*

Input Voltage (Vin) . . . . . -1.0V to +7.0V
Output Voltage (Vout) . . . . . -1.0V to +7.0V
Power Supply Voltage (VCC) . . . . . -1.0V to +7.0V
Operating Temperature (T_{OPR}) . . . . . 0°C to +70°C
Storage Temperature (T_{STG}) . . . . . -55°C to +150°C
Soldering Temperature X Time (T_{SLODER}) . . . . . 260°C X 10sec
Power Dissipation (P_D) 1W
Short Circuit Output Current (Iout) 50mA
Latch-up Current 200mA

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of these specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (VCC = 5V ± 10%, VSS = 0V, Ta = 0°C to +70°C)

Symbol	Parameter	-40		-50		-60		Unit	Test Conditions	Notes
		Min.	Max.	Min.	Max.	Min.	Max.			
I_{IL}	Input Leakage Current	-10	+10	-10	+10	-10	+10	µA	0V ≤ Vin ≤ +5.5V Pins not under Test = 0V	
I_{OL}	Output Leakage Current	-10	+10	-10	+10	-10	+10	µA	DOUT disabled, 0V ≤ Vout ≤ +5.5V	
I_{CC1}	Operating Power Supply Current	-	160	-	140	-	120	mA	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ Address cycling; t_{RC} = min.	1, 2
I_{CC2}	TTL Standby Power Supply Current	-	3.0	-	3.0	-	3.0	mA	$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$ =V_{IH}	
I_{CC3}	Average Power Supply Current, $\overline{RAS}$ Refresh Mode	-	160	-	140	-	120	mA	$\overline{RAS}$ cycling, $\overline{UCAS}$=$\overline{LCAS}$ = V_{IH}, t_{RC} = min.	1
I_{CC4}	Fast Page Mode Average Power Supply Current	-	160	-	140	-	120	mA	$\overline{RAS}$ = V_{IL}, $\overline{UCAS}$, $\overline{LCAS}$ Address cycling; t_{PC} = min.	1, 2
I_{CC5}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Power Supply Current	-	160	-	140	-	120	mA	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ cycling; t_{RC} = min.	1
I_{CC6}	CMOS Standby Power Supply Current	-	2.0	-	2.0	-	2.0	mA	$\overline{RAS}$=$\overline{UCAS}$=$\overline{LCAS}$ = VCC - 0.2V	
V_{OH}	Output Voltage	2.4	-	2.4	-	2.4	-	V	I_{OUT} = -5.0mA	
V_{OL}		-	0.4	-	0.4	-	0.4	V	I_{OUT} = 4.2mA	

AC Characteristics (VCC = 5V ± 10%, VSS = 0V, Ta = 0°C to +70°C)

#	JEDEC Symbol	Std Symbol	Parameter	-40		-50		-60		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL2RL2}	t_{RC}	Random Read or Write Cycle Time	75	-	90	-	110	-	ns	
2	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	25	-	25	-	25	-	ns	
3	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	40	75K	50	75K	60	75K	ns	
4	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	12	-	12	-	12	-	ns	
5	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	16	30	18	37	20	45	ns	6
6	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	11	22	13	25	15	30	ns	7
7	t_{CL1RH1}	$t_{RSH(R)}$	$\overline{CAS}$ to $\overline{RAS}$ Hold Time (Read)	12	-	12	-	12	-	ns	
8	t_{RL1CH1}	t_{CSH}	$\overline{RAS}$ to $\overline{CAS}$ Hold Time	40	-	50	-	60	-	ns	
9	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
10	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0	-	0	-	0	-	ns	
11	t_{RL1AX}	t_{RAH}	Row Address Hold Time	6	-	8	-	10	-	ns	
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	4, 5
	t_{RVRV}	t_{REF}	Refresh Period	-	4	-	4	-	4	ms	3
12	t_{CL1QX}	t_{CLZ}	$\overline{CAS}$ to Output in Low Z	0	-	0	-	0	-	ns	8

Read Cycle (VCC = 5V ± 10%, VSS = 0V, Ta = 0°C to +70°C)

#	JEDEC Symbol	Std Symbol	Parameter	-40		-50		-60		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
13	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$	-	40	-	50	-	60	ns	6
14	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$	-	12	-	13	-	15	ns	6, 13
15	t_{AVQV}	t_{AA}	Access Time from Address	-	20	-	25	-	30	ns	7, 13
16	t_{RL1AZ}	$t_{AR(R)}$	Column Add Hold from $\overline{RAS}$	30	-	40	-	45	-	ns	
17	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0	-	0	-	0	-	ns	
18	t_{CH2WX}	t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	-	0	-	0	-	ns	9
19	t_{RH2WX}	t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	-	0	-	0	-	ns	9
20	t_{AVRH1}	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	20	-	25	-	30	-	ns	
21	t_{CH2CL2}	t_{CRP}	$\overline{CAS}$ Precharge Time	5	-	5	-	5	-	ns	
22	t_{RH2OL1}	t_{ODS}	Output Disable Setup Time	0	-	0	-	0	-	ns	
23	t_{CH2QZ}	t_{OFF}	Output Buffer Turn-Off Time	0	8	0	10	0	12	ns	8, 10

Write Cycle (VCC = 5V ± 10%, VSS = 0V, Ta = 0°C to +70°C)

#	JEDEC Symbol	Std Symbol	Parameter	-40		-50		-60		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
24	t_{AVWL2}	t_{ASC}	Column Address Setup Time	0	-	0	-	0	-	ns	
25	t_{1CL1AX}	t_{CAH}	Column Address Hold Time	6	-	8	-	10	-	ns	
26	t_{RL1AX}	t_{AWR}	Column Address Hold Time to $\overline{RAS}$	30	-	40	-	45	-	ns	
27	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0	-	0	-	0	-	ns	11
28	t_{CH2WH1}	t_{WCH}	Write Command Hold Time	6	-	7	-	10	-	ns	11
29	t_{RL1WH1}	t_{WCR}	Write Command Hold Time to $\overline{RAS}$	30	-	40	-	45	-	ns	
30	t_{WL1WH1}	t_{WP}	Write Command Pulse Width	6	-	7	-	10	-	ns	
31	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	12	-	13	-	15	-	ns	
32	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	12	-	13	-	15	-	ns	
33	t_{DVWL2}	t_{DS}	Data-in setup Time	0	-	0	-	0	-	ns	12
34	t_{WL1DX} t_{CL1DX}	t_{DH}	Data-in Hold Time	6	-	7	-	10	-	ns	12
35	t_{RL1DX}	t_{DHR}	Data-in Hold Time to $\overline{RAS}$	33	-	40	-	45	-	ns	

Read-Modify-Wirte Cycle (VCC = 5V ± 10%, VSS = 0V, Ta = 0°C to +70°C)

#	JEDEC Symbol	Std Symbol	Parameter	-40		-50		-60		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
36	t_{RL2RL2}	t_{RWC}	Read-Modify-Write Cycle Time	120	-	130	-	140	-	ns	
37	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	63	-	75	-	85	-	ns	11
38	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	30	-	33	-	38	-	ns	11
39	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay Time	38	-	43	-	53	-	ns	11
40	t_{CL1RH1}	$t_{RSH(W)}$	$\overline{CAS}$ to $\overline{RAS}$ Hold Time (Write)	12	-	12	-	12	-	ns	
41	t_{CL1CH1}	$t_{CAS(W)}$	$\overline{CAS}$ Pulse Width (Write)	12	-	12	-	12	-	ns	

Fast Page Mode Cycle (VCC = 5V ± 10%, VSS = 0V, Ta = 0°C to +70°C)

#	JEDEC Symbol	Std Symbol	Parameter	-40		-50		-60		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
42	t_{AVAV} t_{WL2WL2}	t_{PC}	Read-Write Cycle Time (Fast Page)	22	-	31	-	40	-	ns	14
43	t_{CH2CQV}	t_{CPA}	Access Time from $\overline{CAS}$ Precharge	-	25	-	30	-	35	ns	13
44	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page)	7	-	8	-	10	-	ns	
45	t_{CL2CL2}	t_{PCM}	FAST PAGE Mode RMW Cycle	55	-	63	-	85	-	ns	
46	t_{CL2CH2}	t_{CRW}	Page Mode $\overline{CAS}$ Pulse Width (RMW)	45	-	49	-	60	-	ns	
47	t_{RLRH1}	t_{RASP}	$\overline{RAS}$ Pulse Width	40	125K	50	125K	60	125K	ns	

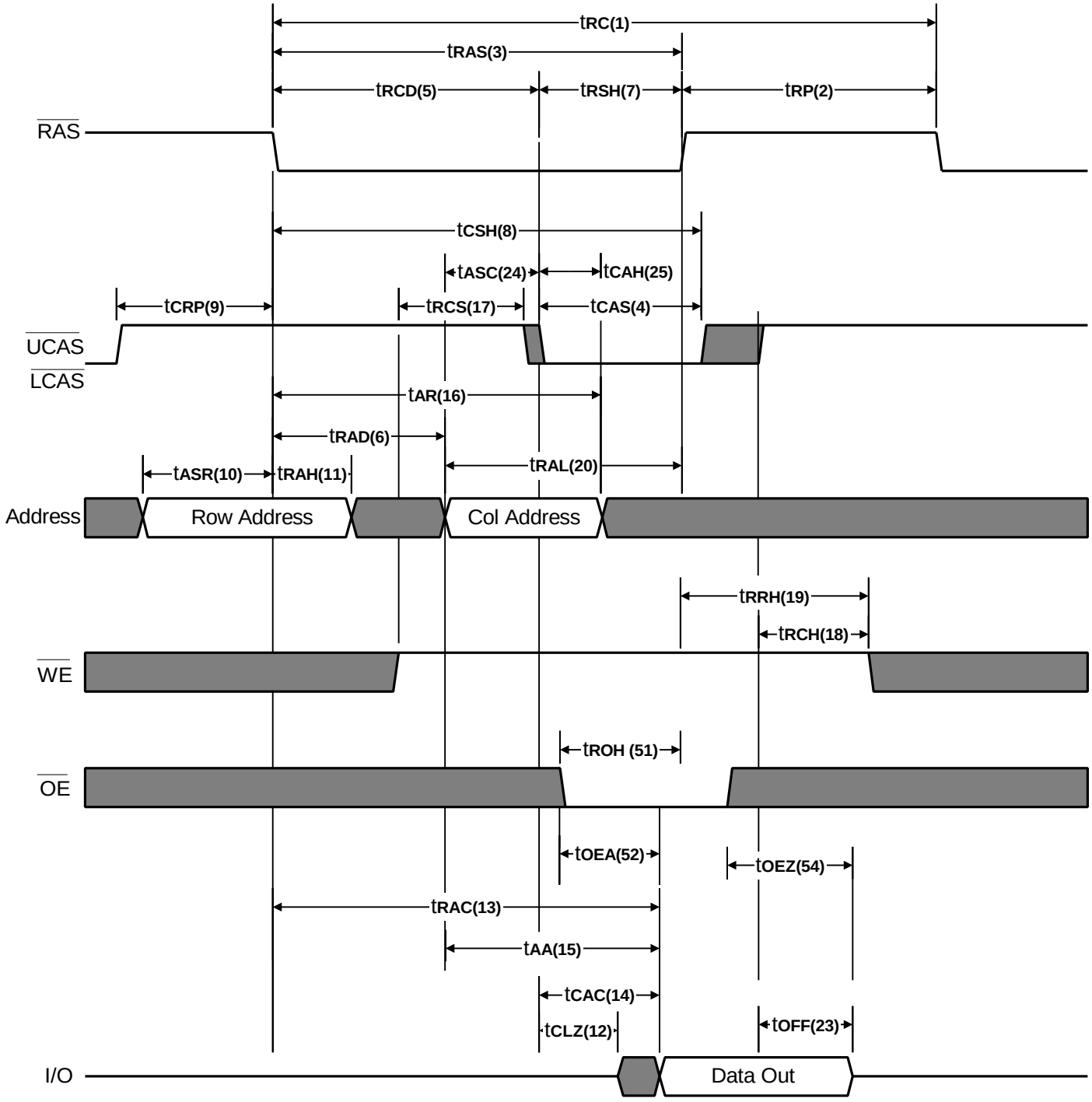
Refresh Cycle (VCC = 5V ± 10%, VSS = 0V, Ta = 0°C to +70°C)

#	JEDEC Symbol	Std Symbol	Parameter	-40		-50		-60		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
48	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$-before-$\overline{RAS}$)	5	-	5	-	5	-	ns	3
49	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$-before-$\overline{RAS}$)	10	-	10	-	10	-	ns	3
50	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	-	5	-	5	-	ns	
51	t_{OL1RH1}	t_{ROH}	$\overline{RAS}$ Hold Time Reference to $\overline{OE}$	5	-	5	-	5	-	ns	
52	t_{OL1QV}	t_{OEA}	$\overline{OE}$ Access Time	-	12	-	13	-	15	ns	
53	t_{OH2QX}	t_{OED}	$\overline{OE}$ to Data Delay	8	-	10	-	13	-	ns	
54	t_{OH2QZ}	t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$	0	8	0	10	0	13	ns	8
55	t_{WL1OL2}	t_{OEH}	$\overline{OE}$ Command Hold Time	0	-	0	-	0	-	ns	

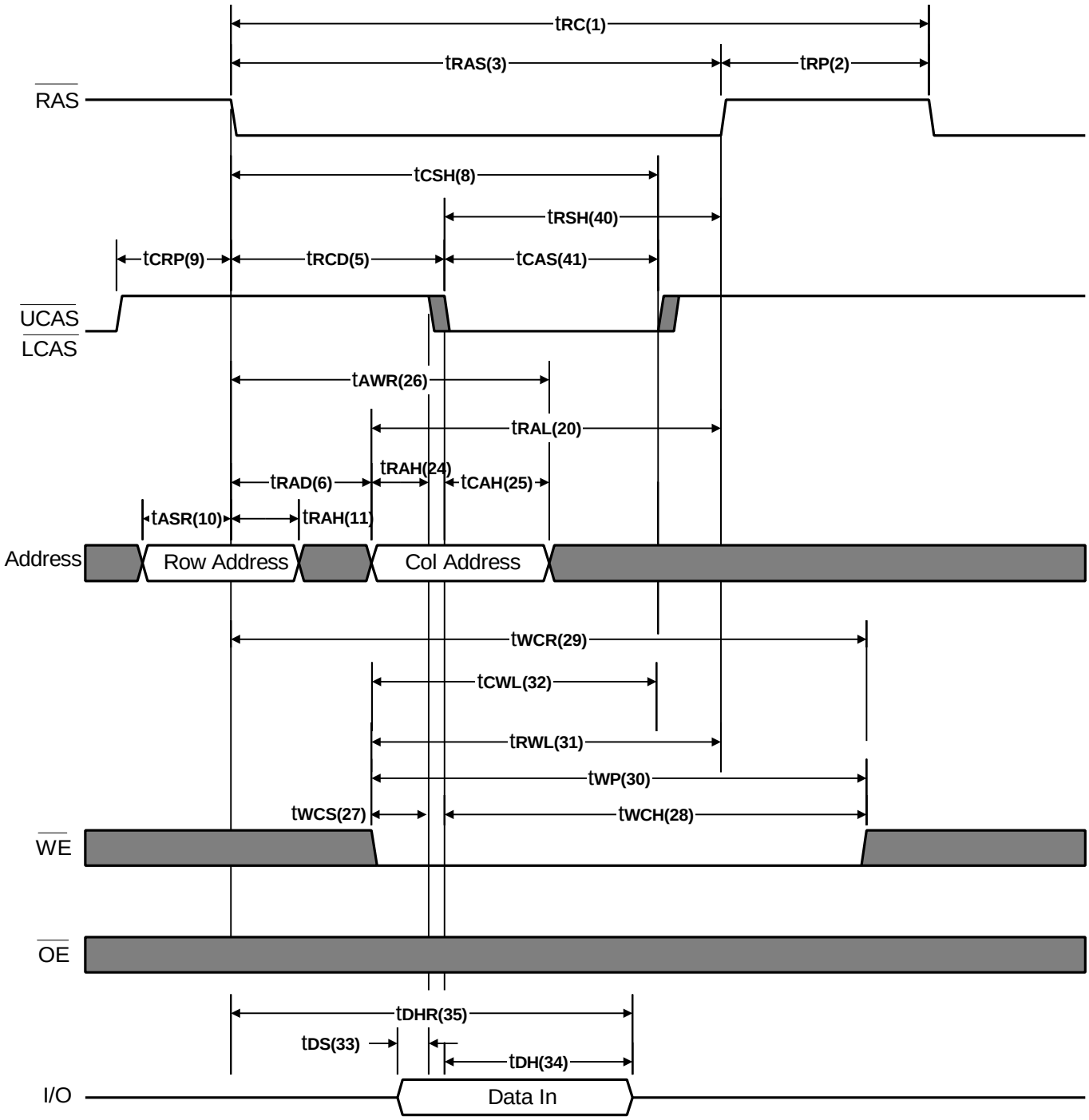
Notes:

1. I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. An initial pause of 200µs is required after power-up followed by any 8 $\overline{RAS}$ cycles before proper device operation is achieved. In the case of an internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required. 8 initialization cycles are required after extended periods of bias without clocks (greater than 8ms).
4. AC Characteristics assume t_T = 5ns. All AC parameters are measured with a load equivalent to two TTL loads and 100pF, V_{IL} (min.) ≥ GND and V_{IH} (max.) ≤ VCC.
5. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
6. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
7. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
8. Assumes three state test load (5pF and a 380Ω Thevenin equivalent).
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition; it is not referenced to output nvoltage levels.
11. t_{WCS}, t_{WCH}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If t_{WCS} ≥ t_{WCS} (min.) and t_{WCH} ≥ t_{WCH} (min.), the cycle is an early write cycle and data out pins will remain open circuit, high impedance, throughout the cycle. If t_{RWD} ≥ t_{RWD} (min.) , t_{CWD} ≥ t_{CWD} (min.) and t_{AWD} ≥ t_{AWD} (min.), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out at access time is indeterminate.
12. These parameters are referenced to $\overline{UCAS}$ and $\overline{LCAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in read-write cycles.
13. Access time is determined by the longest of t_{AA} or t_{CAC} or t_{CAP}.
14. t_{ASC} ≥ t_{CP} to achieve t_{PC} (min.) and t_{CAP} (max.) values.
15. These parameters are sampled and not 100% tested.

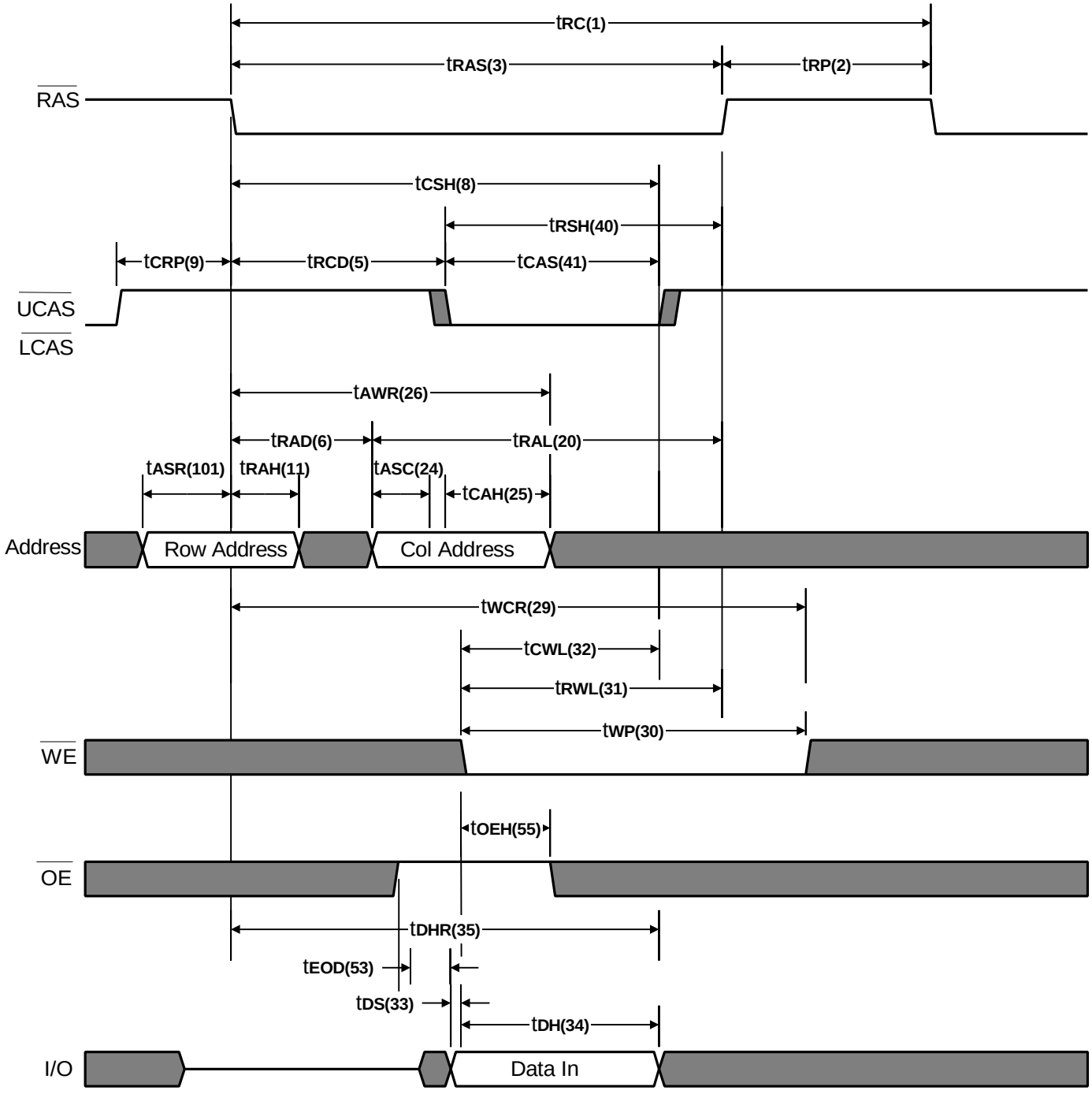
Timing Waveform of Read Cycle



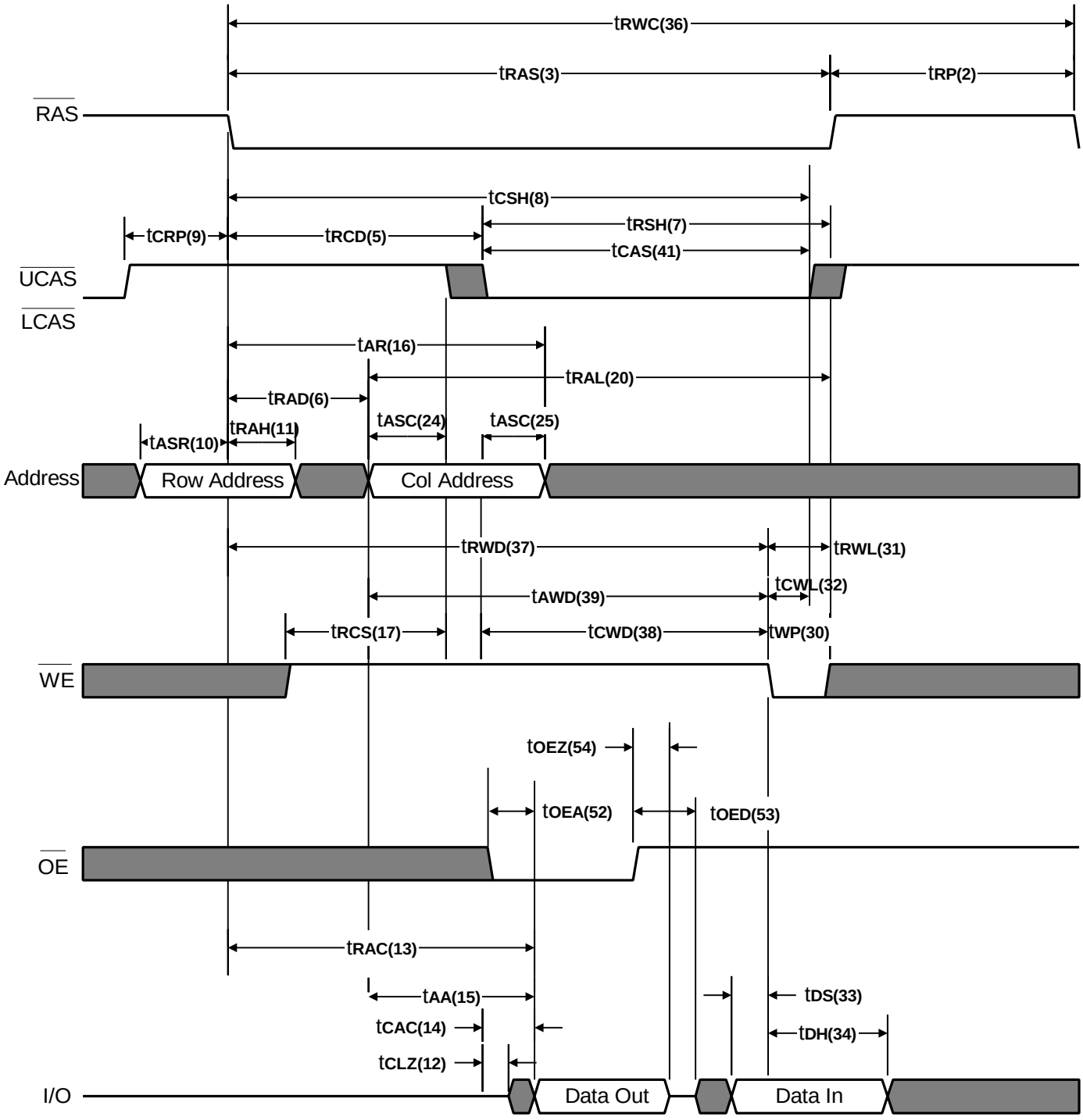
Timing Waveform of Early Write Cycle



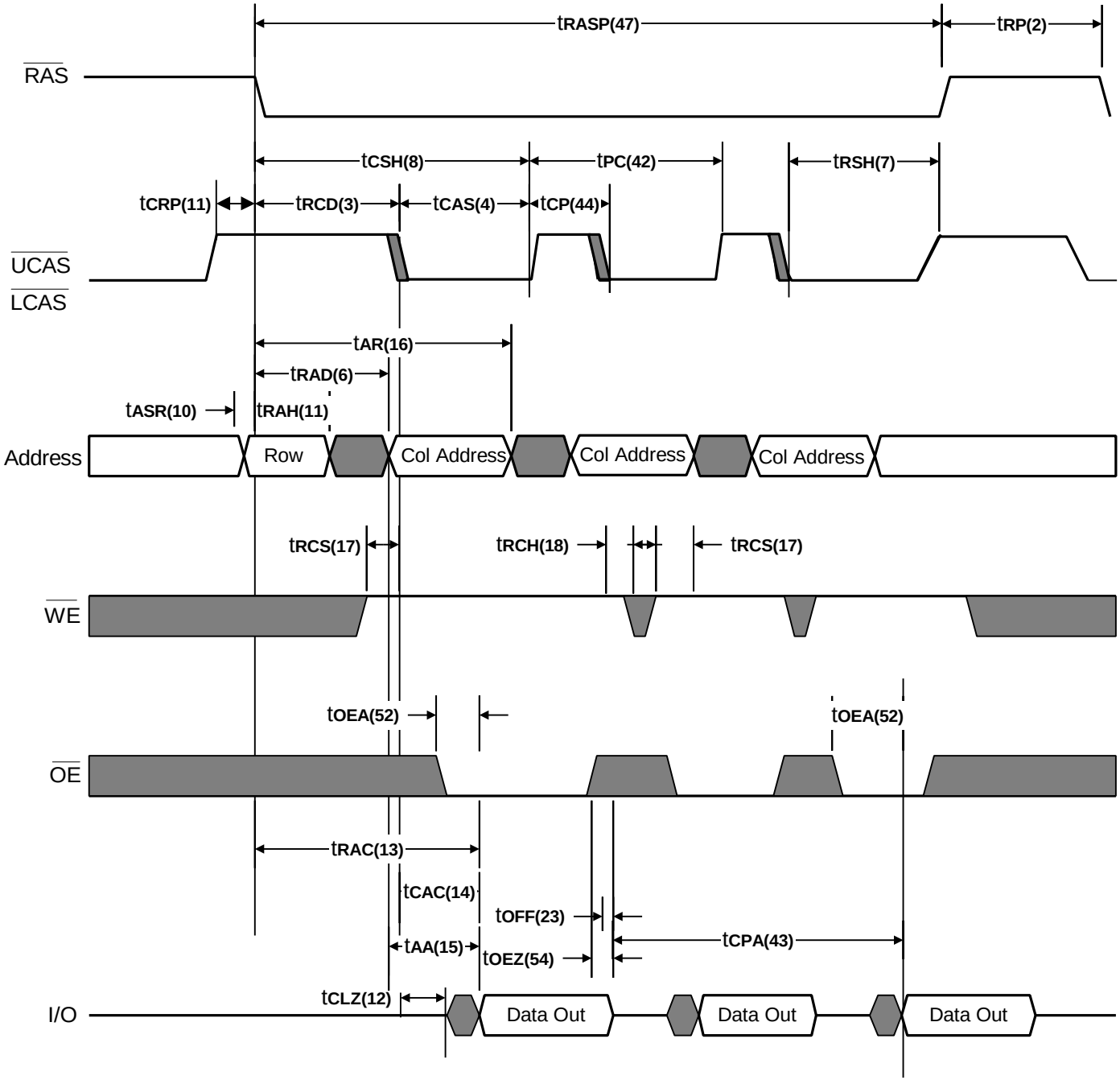
Timing Waveform of Late Write Cycle



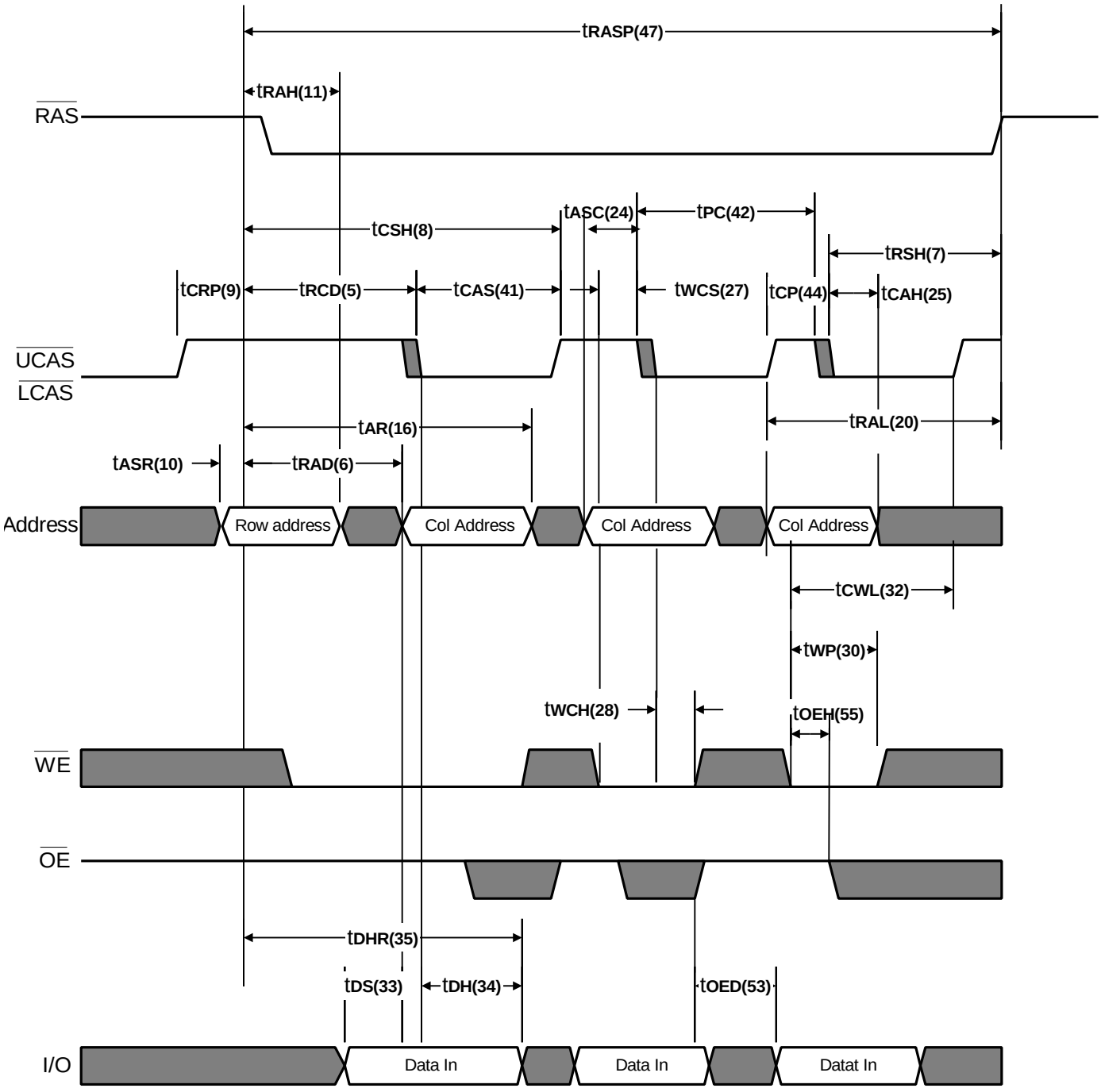
Timing Waveform of Read-Modify-Write Cycle



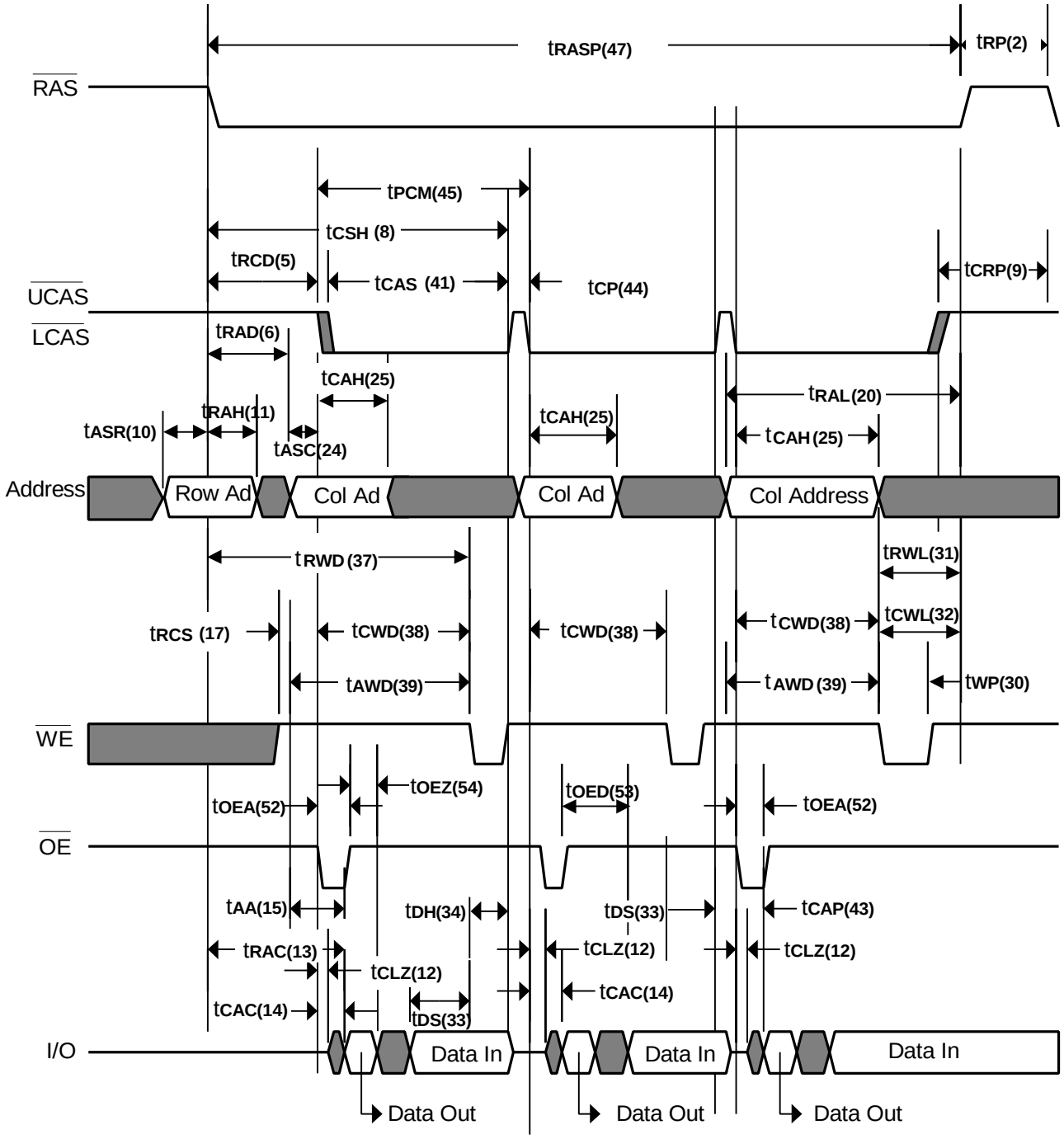
Timing Waveform of Fast Page Mode Read Cycle



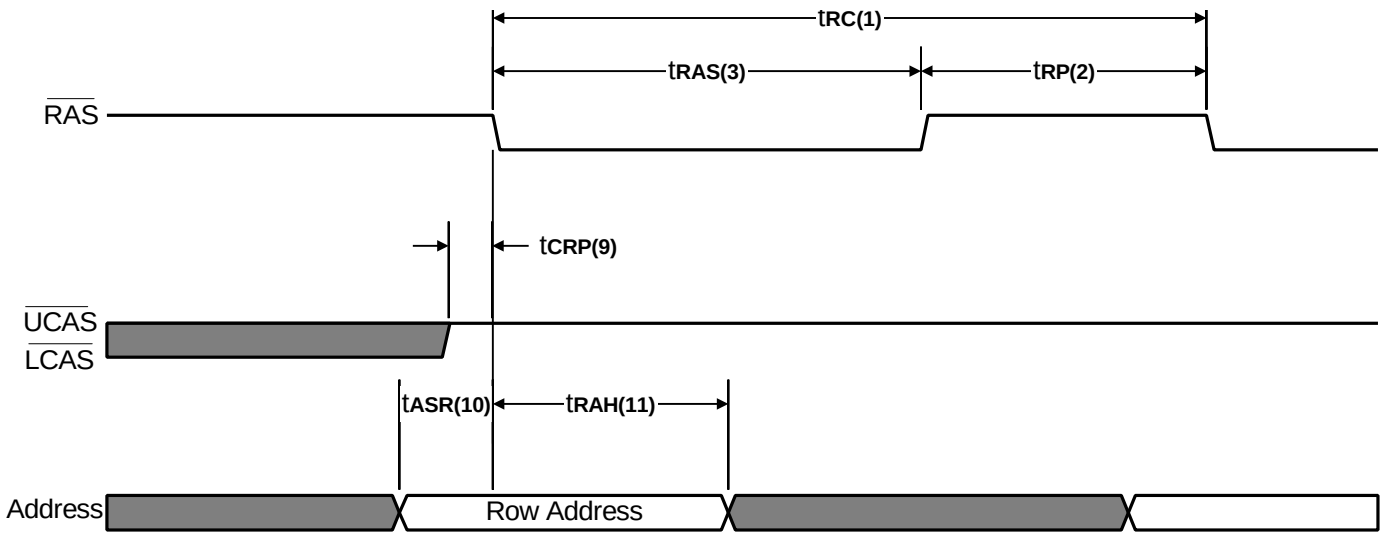
Timing Waveform of Fast Page Mode Early Write Cycle



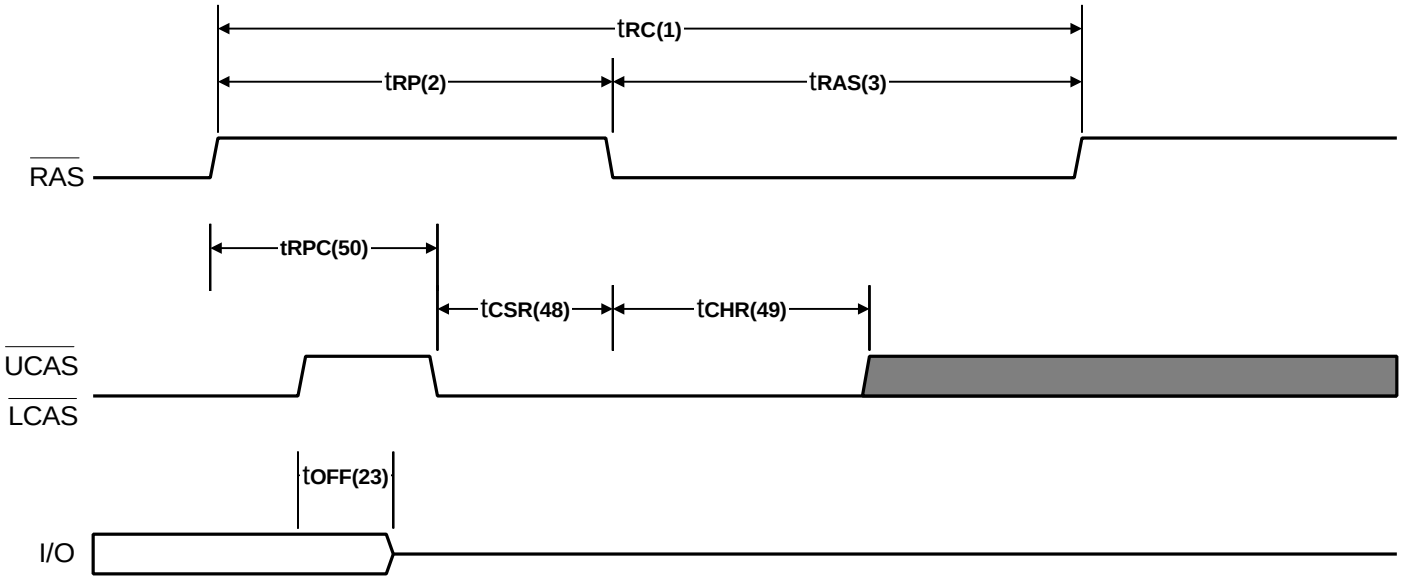
Timing Waveform of Fast Page Mode Read-Modify-Write Cycle



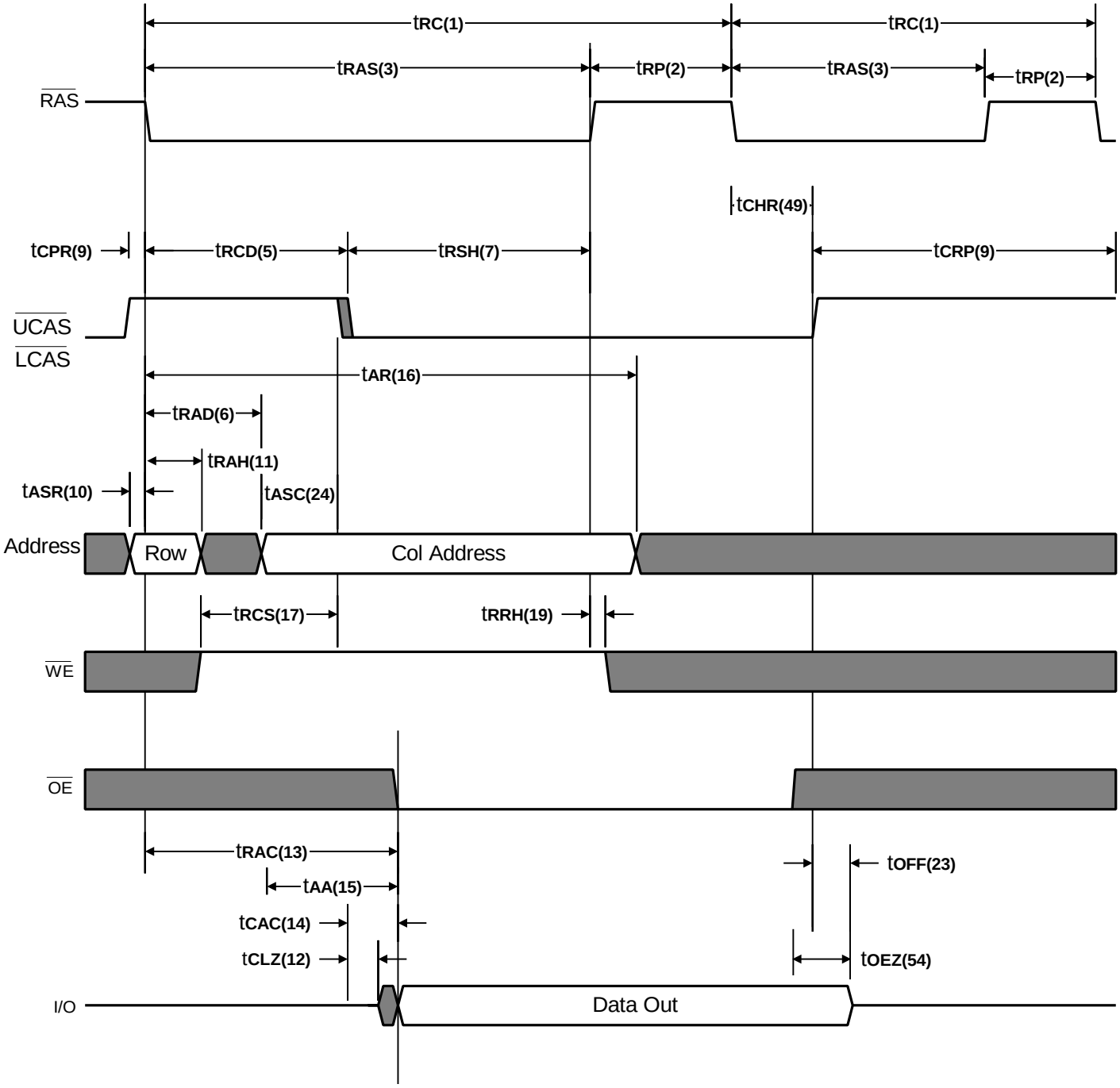
Timing Waveform of $\overline{RAS}$ Only Refresh Cycle



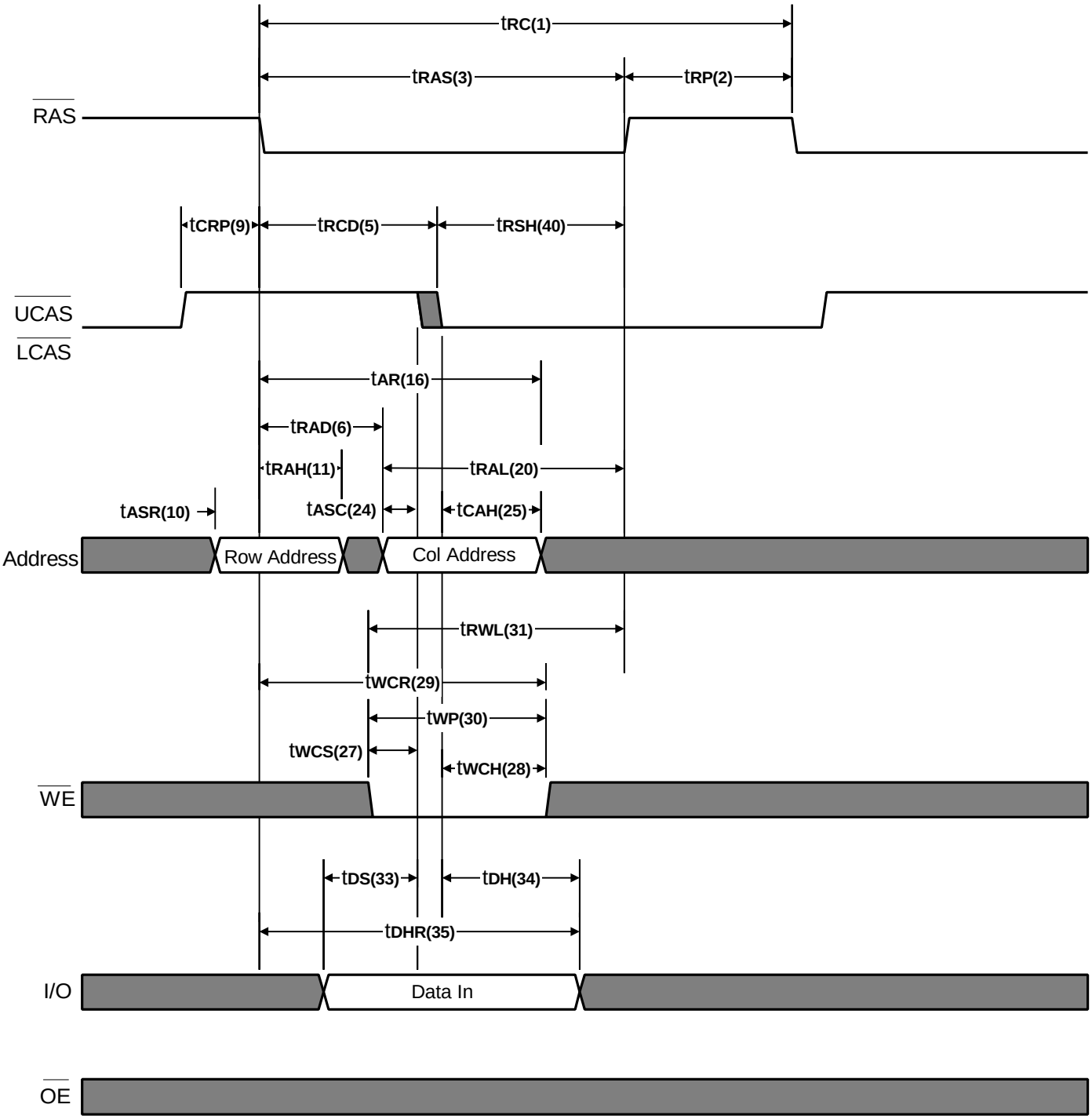
Timing Waveform of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



Timing Waveform of Hidden Refresh Cycle (Read)



Timing Waveform of Hidden Refresh Cycle (Write)



Capacitance[15] (f = 1MHz, Ta = Room Temperature, VCC = 5V ± 10%)

Symbol	Signals	Parameter	Max.	Unit	Test Conditions
C_{IN1}	A0 – A7	Input Capacitance	5	pF	Vin = 0V
C_{IN2}	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$		7	pF	Vin = 0V
$C_{I/O}$	I/O_1 - I/O_{16}	I/O Capacitance	7	pF	Vin = Vout = 0V

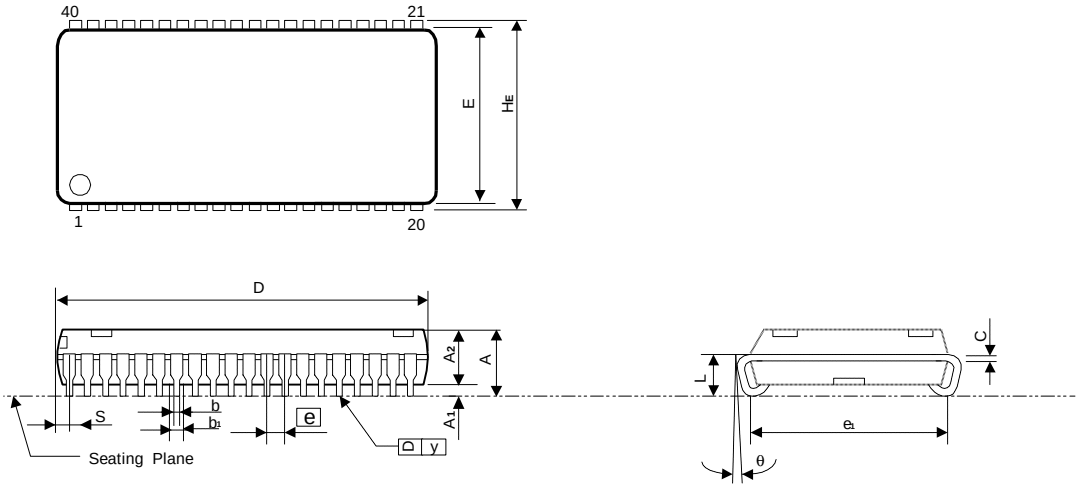
Ordering Codes

Package\ $\overline{RAS}$ Access Time	40ns	50ns	60ns
40L SOJ (400 mil)	A416316S-40	A416316S-50	A416316S-60
40/44L TSOP type II (400mil)	A416316V-40	A416316V-50	A416316V-60

Package Information

SOJ 40L Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.144	-	-	3.66
A_1	0.025	-	-	0.64	-	-
A_2	0.105	0.110	0.115	2.67	2.79	2.92
b_1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
C	0.008	0.010	0.014	0.20	0.25	0.36
D	1.020	1.025	1.030	25.91	26.04	26.16
E	0.395	0.400	0.405	10.03	10.16	10.29
e	0.044	0.050	0.056	1.12	1.27	1.42
e_1	0.355	0.366	0.376	9.114	9.383	9.652
H_E	0.430	0.440	0.450	10.92	11.18	11.43
L	0.081	0.093	0.105	2.083	2.39	2.70
S	-	-	0.050	-	-	1.27
y	-	-	0.004	-	-	0.10
θ	0°	-	10°	0°	-	10°

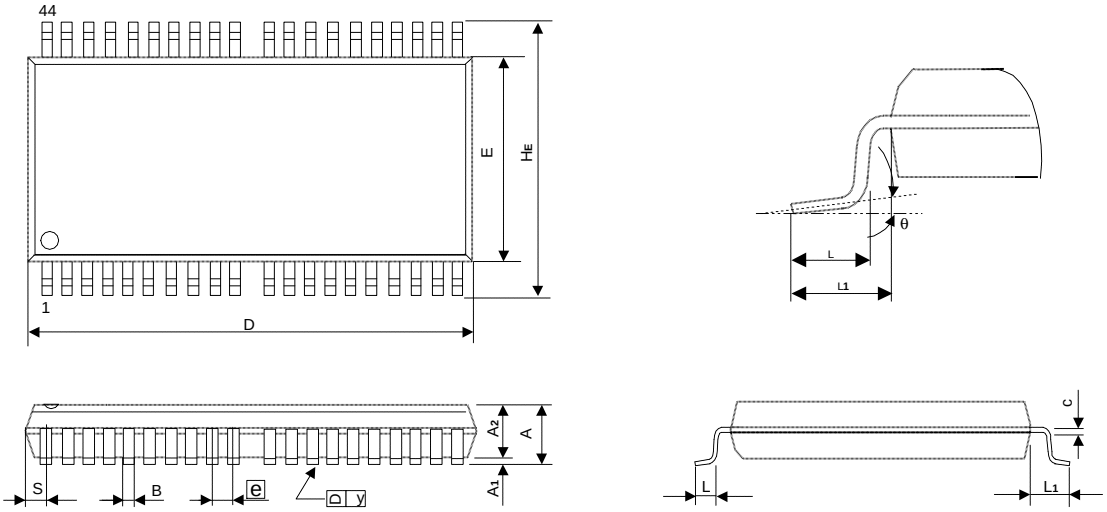
Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

Package Information

TSOP 40/44L (Type II) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A_2	0.037	0.039	0.041	0.95	1.00	1.05
B	0.013	0.015	0.017	0.32	0.37	0.42
c	0.003	0.005	0.009	0.08	0.13	0.23
D	0.720	0.725	0.730	18.28	18.41	18.54
E	0.395	0.400	0.405	10.03	10.16	10.29
e	0.031 BSC			0.80 BSC		
H_E	0.455	0.463	0.471	11.56	11.76	11.96
L	0.016	0.020	0.024	0.40	0.50	0.60
L_1	-	0.031	-	-	0.80	-
S	-	-	0.035	-	-	0.90
y	-	-	0.004	-	-	0.10
θ	1°	3°	5°	1°	3°	5°

Notes:
1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.